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Amendments to the Claims

Please amend the claims as set forth in the following listing. This listing of claims will replace all prior versions, and listings, of claims for the present application:

1. (Currently amended) An antenna error detection and circuit protection system, comprising:
a current limit detection circuit integrated within an integrated radio receiver and configured to detect current levels drawn by at least one antenna mounted remotely from the integrated radio receiver, the current limit detection circuit having a gate drive signal as an output; and
a current limiting pass transistor having its source and drain coupled between a supply voltage and an antenna and having its gate coupled to the gate drive signal;
wherein the current limit detection circuit is configured to adjust the gate drive signal to reduce current flow through the pass transistor when the detected current level drawn by the at least one antenna rises above a current limit level;
wherein a terrestrial antenna and a satellite antenna are coupled to the current limit detection circuit and to the current limiting pass transistor.

2. (Original) The system of claim 1, wherein the current limiting pass transistor is an external transistor device.

3. (Original) The system of claim 1, wherein the current limiting pass transistor is a transistor device integrated within the integrated radio receiver.

4. (Original) The system of claim 1, further comprising a voltage protection device coupled between the current limiting transistor and the at least one antenna.

5. (CANCELLED) The system of claim 1, wherein a terrestrial antenna and a satellite antenna are coupled to the current limit detection circuit and to the current limiting pass transistor.

6. (Currently amended) The system of ~~claim 5~~ claim 1, wherein the integrated radio receiver includes a terrestrial antenna input pin, a satellite antenna input pin, and an antenna sense input pin, and wherein the terrestrial antenna is coupled to the terrestrial antenna input pin, the satellite antenna is coupled to the

satellite antenna input pin, and the terrestrial and satellite antennas are both coupled to the antenna sense input pin.

7. (Original) The system of claim 6, wherein the terrestrial and satellite antennas are coupled to the antenna sense input pin through a first and second resistors.

8. (Original) The system of claim 7, wherein the first and second resistors are matched and are selected to determine the current limit level.

9. (Original) The system of claim 6, wherein a first circuit protection resistor is coupled to the terrestrial antenna input pin, a second circuit protection resistor is coupled to the satellite antenna input pin, and a third protection resistor is coupled to the antenna sense input pin.

10. (Original) The system of claim 9, wherein the first circuit protection resistor is coupled between the terrestrial antenna and the terrestrial antenna input pin, the second circuit protection resistor is coupled between the satellite antenna and the satellite antenna input pin, and the third protection resistor is coupled between the terrestrial and satellite antennas and the antenna sense input pin

11. (Original) The system of claim 10, wherein the first, second and third resistors are matched.

12. (Original) The system of claim 6, wherein on-chip current sinks are coupled to each of the terrestrial antenna input pin, the satellite antenna input pin, and the antenna sense input pin.

13. (Original) The system of claim 6, wherein at least one on-chip protection diode is coupled to the terrestrial antenna input pin, at least one on-chip protection diode is coupled to the satellite antenna input pin, and at least one on-chip protection diode is coupled to the antenna sense input pin.

14. (Currently amended) An antenna error detection and circuit protection system, comprising:

a current and voltage detection circuit integrated within an integrated radio receiver and configured to detect current and voltage levels drawn by at least one antenna mounted remotely from the integrated radio receiver, the current and voltage detection circuit configured to determine under-current, over-current, and over-voltage antenna error conditions; and at least one antenna error output pin for the integrated radio receiver, the antenna error output pin providing an output signal indicative of an antenna error condition;

wherein a terrestrial antenna and a satellite antenna are coupled to the current and voltage detection circuit, the current and voltage detection circuit being configured to determine under-current, over-current, and over-voltage antenna error conditions for the terrestrial antenna and the satellite antenna.

15. (Original) The system of claim 14, wherein the antenna error output pin is configured to transition from a first logic state to a second logic state upon an occurrence of an antenna error condition.

16. (Original) The system of claim 14, wherein the current and voltage detection circuit is configured to provide error flags for an on-chip register within the integrated radio receiver, the error flags being configured to represent an occurrence of the under-current, over-current, and over-voltage antenna error conditions.

17. (CANCELLED) The system of claim 14, wherein a terrestrial antenna and a satellite antenna are coupled to the current and voltage detection circuit, the current and voltage detection circuit being configured to determine under-current, over-current, and over-voltage antenna error conditions for the terrestrial antenna and the satellite antenna.

18. (Currently amended) The system of ~~claim 17~~ claim 14, wherein the integrated radio receiver includes a terrestrial antenna input pin, a satellite antenna input pin, and an antenna sense input pin, and wherein the terrestrial antenna is coupled to the terrestrial antenna input pin, the satellite antenna is coupled to the satellite antenna input pin, and the terrestrial and satellite antennas are both coupled to the antenna sense input pin.

19. (Original) The system of claim 18, wherein a first circuit protection resistor is coupled to the terrestrial antenna input pin, a second circuit protection resistor is coupled to the satellite antenna input pin, and a third protection resistor is coupled to the antenna sense input pin.

20. (Original) The system of claim 19, wherein the protection resistors are integrated within the integrated radio receiver.

21. (Currently amended) The system of ~~claim 17~~ claim 14, wherein a first antenna error output pin is configured to transition from a first logic state to a second logic state upon an occurrence of the terrestrial antenna error condition, and a second antenna error output pin is configured to transition from a first logic state to a second logic state upon an occurrence of the satellite antenna error condition.

22. (Original) The system of claim 21, wherein the current and voltage detection circuit is configured to provide error flags for an on-chip register within the integrated radio receiver, the error flags being configured to represent an occurrence of the under-current, over-current, and over-voltage antenna error conditions for the terrestrial antenna and the satellite antenna.

23. (Currently amended) The system of ~~claim 17~~ claim 14, wherein three output pins for the integrated radio receiver are configured to provide a 3-bit output signal, the 3-bit output signal identifying what antenna error condition has occurred upon occurrence of an under-current, over-current, and over-voltage antenna error.

24. (Original) The system of claim 23, wherein at least one of the three output pins are utilized for dual purposes for the integrated radio receiver.

25. (Original) The system of claim 24, wherein at least two of the three pins are utilized to provide at least part of a serial interface.

26. (Original) The system of claim 24, wherein at least one of the three pins is utilized to provide a reset signal to an external frequency synthesizer circuit.

27. (Currently amended) A method for detecting errors in and protecting antenna circuitry, comprising:

detecting current levels drawn by at least one antenna mounted remotely from the integrated radio receiver;

generating a gate drive signal based upon the detected current levels;

controlling current through a current limiting pass transistor with the gate drive signal, the current limiting pass transistor having its source and drain coupled between a supply voltage and an antenna and having its gate coupled to the gate drive signal; and

adjusting the gate drive signal to reduce current flow through the pass transistor when the detected current level drawn by the at least one antenna rises above a current limit level;

wherein a terrestrial antenna and a satellite antenna are coupled to the current limiting pass transistor.

28. (Original) The method of claim 27, wherein the current limiting pass transistor is an external transistor device.

29. (Original) The method of claim 27, wherein the current limiting pass transistor is a transistor device integrated within the integrated radio receiver.

30. (Original) The method of claim 27, further comprising providing a voltage protection device coupled between the current limiting transistor and the at least one antenna.

31. (CANCELLED) The method of claim 27, wherein a terrestrial antenna and a satellite antenna are coupled to the current limiting pass transistor.

32. (Currently amended) A method for detecting errors in and protecting antenna circuitry, comprising:

detecting current levels drawn by at least one antenna mounted remotely to an integrated radio receiver to determine under-current, over-current, and over-voltage antenna error conditions;

detecting voltage levels drawn by at least one antenna mounted remotely from the integrated radio receiver to determine under-current, over-current, and over-voltage antenna error conditions; and

utilizing at least one antenna error output pin for the integrated radio receiver to provide an output signal indicative of an antenna error condition;

wherein a terrestrial antenna and a satellite antenna are coupled to the integrated radio receiver and wherein the detecting steps comprise detecting current and voltage levels for both the terrestrial antenna and the satellite antenna.

33. (Original) The method of claim 32, further comprising transitioning the antenna error output pin from a first logic state to a second logic state upon an occurrence of an antenna error condition.

34. (Original) The method of claim 32, further comprising generating error flags for an on-chip register within the integrated radio receiver, the error flags being configured to represent an occurrence of the under-current, over-current, and over-voltage antenna error conditions.

35. (CANCELLED) The method of claim 32, wherein a terrestrial antenna and a satellite antenna are coupled to the integrated radio receiver and wherein the detecting steps comprise detecting current and voltage levels for both the terrestrial antenna and the satellite antenna.

36. (Currently amended) The method of ~~claim 35~~ claim 32, further comprising utilizing a first antenna error output pin to indicate an occurrence of a terrestrial antenna error condition, and a second antenna error output pin to indicate an occurrence of a satellite antenna error condition.

37. (Currently amended) The method of ~~claim 35~~ claim 32, further comprising generating error flags for an on-chip register within the integrated radio receiver, the error flags being configured to represent an occurrence of the under-current, over-current, and over-voltage antenna error conditions for the terrestrial antenna and the satellite antenna.

38. (Original) The method of claim 32, utilizing three output pins for the integrated radio receiver to provide a 3-bit output signal, the 3-bit output signal identifying what antenna error condition has occurred upon occurrence of an under-current, over-current, and over-voltage antenna error.

39. (Original) The system of claim 38, wherein at least one of the three output pins are utilized for dual purposes for the integrated radio receiver.